AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (currently amended): A semiconductor memory device which has a redundancy circuit, the semiconductor memory device comprising:

a plurality of memory blocks; and

a plurality of redundancy memory blocks provided for each of said plurality of memory blocks,

wherein each of said plurality of memory blocks includes a plurality of segments,

said plurality of segments are adjacent to one after another, and

segments having defects among said plurality of segments in a memory block among said plurality of memory blocks are ~~dispersively~~ sequentially allocated to said plurality of redundancy memory blocks and replaced by said allocated redundancy memory blocks~~, and~~

~~each of said plurality of redundancy memory blocks has a redundancy segment which replaces any of the segments having defects~~.

2. (previously presented): The semiconductor memory device according to claim 1,

wherein one each of said plurality of segments includes one or more adjacent memory cell rows or one or more adjacent memory cell columns.

3. (previously presented): The semiconductor memory device according to claim 1,

wherein a position of an address bit for selecting said plurality of memory blocks is different from a position of an address bit for selecting said plurality of redundancy memory blocks.

4. (previously presented): The semiconductor memory device according to claim 3,

wherein address bits that define said plurality of segments are lower address bits, and address bits for selecting said plurality of redundancy memory blocks include an address bit immediately above said lower address bits.

5. (previously presented): A semiconductor memory device comprising:

a memory block having a plurality of segments, each of said plurality of segments including a plurality of memory cells; and

a plurality of redundancy memory blocks which are provided for said memory block,

wherein each of said plurality of redundancy memory blocks has a redundancy segment which substitutes for any segment having a defect among said plurality of segments,

said plurality of segments are allocated to said plurality of redundancy memory blocks,

a number indicating said redundancy memory block allocated to said any segment is given by a remainder generated when an address indicating said any segment is divided by a number of said plurality of redundancy memory blocks, and

each of said plurality of segments is replaceable by said redundancy segment of said allocated redundancy memory block if the each of said plurality of segments has a defect.

6. (previously presented): A semiconductor memory device comprising:

a plurality of memory blocks each of which has a plurality of segments, each of said plurality of segments including a plurality of memory cells; and

a plurality of redundancy memory blocks which are provided for said plurality of memory blocks,

wherein each of said plurality of redundancy memory blocks has a redundancy segment which substitutes for any segment having a defect among said plurality of segments,

said plurality of segments are allocated to said plurality of redundancy memory blocks,

a number indicating said redundancy memory block allocated to said any segment is given by a remainder generated when an address indicating said any segment is divided by a number of said plurality of redundancy memory blocks, and

each of said plurality of segments is replaceable by said redundancy segment of said allocated redundancy memory block if the each of said plurality of segments has a defect.

7. (Cancelled)

8. (previously presented): The semiconductor memory device according to claim 5,

wherein a first segment and a second segment of said plurality of segments are adjacent to each other, and a first redundancy memory block allocated to said first segment and a second redundancy memory block allocated to said second segment are different redundancy memory blocks.

9. (Cancelled)

10. (Cancelled)

11. (previously presented): The semiconductor memory device according to claim 5,

wherein each of said plurality of segments is a group of memory cells connected to 2^n (n=0, 1, 2,...) word lines or bit lines, said word lines are adjacent to one after another when a number of said word lines is plural, and said bit lines are adjacent to one after another when a number of said bit lines is plural.

12. (previously presented): The semiconductor memory device according to claim 5,

wherein a plurality of lower bits of an address for selecting any of said plurality of segments are input to a decode circuit for selecting said redundancy memory blocks.

13. (previously presented): The semiconductor memory device according to claim 6,

wherein a first segment and a second segment of said plurality of segments are adjacent to each other, and a first redundancy memory block allocated to said first segment and a second redundancy memory block allocated to said second segment are different redundancy memory blocks.

14. (previously presented): The semiconductor memory device according to claim 6,

wherein each of said plurality of segments is a group of memory cells connected to 2^n (n=0, 1, 2,...) word lines or bit lines, said word lines are adjacent to one after another when a number of said word lines is plural, and said bit lines are adjacent to one after another when a number of said bit lines is plural.

15. (previously presented): The semiconductor memory device according to claim 6,

wherein a plurality of lower bits of an address for selecting any of said plurality of segments are input to a decode circuit for selecting said redundancy memory blocks.